What Is Claimed Is:

1. A digital-analog converter circuit comprising n serially connected analog switches polarized to match the logic of each data signal n bit (n is an integer of 2 or more), and 2n tone select units respectively connected across the outputs of each of the 2n reference voltage lines.

2. A digital-analog converter circuit as claimed in claim 1 comprising one conductive type MOS transistor, wherein each of said n analog switches corresponds to the logic of each bit of said data signal.

3. A digital-analog converter circuit as claimed in claim 2, wherein the amplitude of said data signal is low by an amount equal to the threshold value of the P channel MOS transistor in the reference voltage level range and is high by an amount equal to the threshold of the N channel MOS transistor.

4. A liquid crystal display device having a first board formed by an effective pixel area comprising a plurality of pixels and a drive circuit containing a digital/analog converter circuit, a second board placed at a specified gap facing said first board, and a liquid crystal layer held between said first and said second boards, wherein

said digital-analog converter circuit comprises an n serially connected analog switches polarized to match the logic of each data signal n bit (n is an integer of 2 or more), and further

comprises 2n tone select units respectively connected across 2n reference voltage lines and pixel section column lines.

5. A liquid crystal display device as claimed in claim 4, wherein each pixel of said effective pixel area is driven by a common inversion method to invert at each one horizontal period, a common voltage jointly applied to the electrodes of the liquid crystal cell.

6. A liquid crystal display device as claimed in claim 4 comprising a shift register comprising a plurality of transfer stages to output sampling pulses in sequence from each transfer stage by performing shift operation in response to a start signal, a first latch circuit to synchronize with the sampling pulse output from each transfer stage of said shift registers, and sequentially sample and latch the data signals, and a second latch circuit to latch the signal sampled in said first latch circuit with the matching column line at each one horizontal period and supply said latched signal to said digital/analog conversion circuit, and besides

said shift register having a first level shift circuit to supply said start signal to the initial stage of the transfer stages and a second level shift circuit to supply clock signals to each of the transfer stages as a level shift, the first and second level shift circuits have a CMOS latch cell as a basic structure and resistor elements inserted between the two input

sections and two input signal sources of the said CMOS latch cell and,

said first latch circuit having a CMOS latch cell as a basic structure has a first switch connected between the two input sections and two input signal sources of the said CMOS latch cell, a second switch connected between the power supply line and the power supply side of said CMOS latch cell and, a control means to control the complementary switching of said first and said second switches and,

said second latch circuit having a CMOS latch cell as a basic structure has a first switch and a second switch installed on at least one of the positive power supply or negative power supply side of the CMOS latch to respectively select a first and a second power supply having different power supply voltages and, a control means to control the switching of said first switch and second switches according to each period of the latch operation and output operation of the CMOS latch cell.

7. A liquid crystal display device as claimed in claim 6, wherein said drive circuit has a level shift circuit between said second latch circuit and said digital/analog conversion circuit, to level shift the latched signal in said second latch circuit for output as the level shift to said digital/analog converter circuit and, said level shift circuit has a CMOS latch cell as the basic structure and has resistor elements inserted

respectively between two input signal sources and two input sections of the CMOS latch cell.

8. A liquid crystal display device as claimed in claim 4, wherein each of said n number of analog switches comprises one conductive type MOS transistor corresponding to the logic of each bit of said data signal.

9. A liquid crystal display device as claimed in claim 8, wherein the amplitude of said data signal is as low as the P channel MOS transistor threshold value with respect to the range of the reference voltage level and as high or higher than the N channel MOS transistor threshold value.

10. A level shift circuit having a CMOS latch cell as the basic structure and converting a low voltage amplitude signal to a high voltage amplitude signal, wherein a first resistor element is inserted respectively between the two signal sources and the two input sections of said CMOS latch cell.

11. A level shift circuit as claimed in claim 10, wherein said first resistor element is a transistor.

12. A level shift circuit as claimed in claim 10, wherein a second resistor element is inserted between the power supply and the two input sections of said CMOS latch cell.

13. A level shift circuit as claimed in claim 12, wherein said first resistor element and said second resistor element are transistors.

14. A level shift circuit as claimed in claim 12, wherein level shift operation is performed only when said switch is in on status by utilizing switches having a finite resistance value as said first and said second resistor elements, and at all other times latch operation is performed.

15. A level shift circuit as claimed in claim 14, wherein said level shift circuit has a control circuit to set the switch to on status only when necessary.

16. A level shift circuit as claimed in claim 14, wherein said level shift circuit has a reset circuit to determine the initial status of said CMOS latch cell.

17. A shift register comprising a plurality of transfer stages and having a first level shift circuit to supply a start signal as a level shift to the first stage of the transfer stages and a second level shift circuit to supply a clock signal as a level shift to each of the transfer stages, wherein said first and second level shift circuits have a CMOS latch cell as the basic structure and a first resistor element is inserted respectively between the two input sections and the two input signal sources of said CMOS latch cell.

18. A shift register as claimed in claim 17, wherein said first resistor element is a transistor.

19. A shift register as claimed in claim 17, wherein said second resistor element is inserted respectively between the

power supply and the two input sections of the CMOS latch cell.

20. A shift register as claimed in claim 19, wherein said first and said second resistor elements are transistors.

21. A shift register as claimed in claim 19, wherein level shift operation is performed only when said switch is in on status by utilizing switches having a finite resistance value as said first and said second resistor elements, and at all other times latch operation is performed.

22. A shift register as claimed in claim 21, wherein said shift register has a control circuit to set said switch to on status only when necessary.

23. A shift register as claimed in claim 21, wherein said shift register has a reset circuit to determine the initial status of said CMOS latch cell.

24. A shift register as claimed in claim 17, wherein said shift register is fabricated utilizing thin film transistors formed on a glass substrate.

25. A shift register as claimed in claim 17, wherein said shift register is fabricated utilizing thin film transistors formed on a silicon substrate.

26. A liquid crystal display device which is integrated with a pixel section and drive circuit containing scanning system onto the same substrate, said liquid crystal display device having a scan system comprising a plurality of transfer stages, a first

level shift circuit to supply a start signal as a level shift to the first stage of the transfer stages and a second level shift circuit to supply a clock signal as a level shift to each of the transfer stages, wherein said first and second level shift circuits have a CMOS latch cell as the basic structure and a first resistor element is inserted respectively between the two input sections and the two input signal sources of the CMOS latch cell.

27. A liquid crystal display device as claimed in claim 26, wherein said first resistor element is a transistor.

28. A liquid crystal display device as claimed in claim 26, wherein said second resistor element is inserted respectively between the power supply and the two input sections of the CMOS latch cell.

29. A liquid crystal display device as claimed in claim 28, wherein said first and said second resistor elements are transistors.

30. A liquid crystal display device as claimed in claim 28, wherein level shift operation is performed only when said switch is in on status by utilizing switches having a finite resistance value as said first and said second resistor elements, and at all other times latch operation is performed.

31. A liquid crystal display device as claimed in claim 30, wherein said liquid crystal display device has a control circuit to set said switch to on status only when necessary.

32. A liquid crystal display device as claimed in claim 30, wherein said liquid crystal display device has a reset circuit to determine the initial status of said CMOS latch cell.

33. A liquid crystal display device, wherein said liquid crystal display device has a level shift circuit with a CMOS latch cell as the basic structure and a first resistor element is inserted respectively between the two input sections and the two input signal sources of said CMOS latch cell, and a signal with a low voltage amplitude is converted to a signal with a high voltage amplitude.

34. A liquid crystal display device as claimed in claim 33, wherein said first resistor element is a transistor.

35. A liquid crystal display device as claimed in claim 33, wherein said second resistor element is inserted respectively between the power supply and the two input sections of the CMOS latch cell.

36. A liquid crystal display device as claimed in claim 35, wherein said first and said second resistor elements are transistors.

37. A liquid crystal display device as claimed in claim 35, wherein level shift operation is performed only when said switch is in on status by utilizing switches having a finite resistance value as said first and said second resistor elements, and at all other times latch operation is performed.

38. A liquid crystal display device as claimed in claim 37, wherein said liquid crystal display device has a control circuit to set said switch to on status only when necessary.

39. A liquid crystal display device as claimed in claim 37, wherein said liquid crystal display device has a reset circuit to determine the initial status of said CMOS latch cell.

40. A sampling latch circuit with comparator configuration CMOS latch cell as the basic structure and comprising, a first switch connected respectively between the two input sections and the two input signal sources of said CMOS latch cell and, a second switch connected between the power supply line and the power supply side of said CMOS latch cell and, a control means to control the complementary switching of said first switch and said second switch.

41. A sampling latch circuit as claimed in claim 40, wherein said first switch and said second switch are transistors.

42. A sampling latch circuit as claimed in claim 40, wherein a plurality of said sampling latch circuits are installed and, said second switch is jointly shared by said plurality of sampling latch circuits.

43. A sampling latch circuit as claimed in claim 40 also having a third switch synchronized and controlled by said second switch between the power supply line and the power supply side of the output circuit for output of said CMOS latch circuit output

signal.

44. A sampling latch circuit as claimed in claim 43, wherein said second switch is combined with said third switch.

45. A sampling latch circuit as claimed in claim 44, wherein a plurality of said sampling latch circuits are installed and, said second switch is jointly shared by said plurality of sampling latch circuits.

46. A sampling latch circuit as claimed in claim 40, wherein said sampling latch circuit is fabricated by utilizing thin film transistors formed on a glass substrate.

47. A sampling latch circuit as claimed in claim 40, wherein said sampling latch circuit is fabricated by utilizing thin film transistors formed on a silicon substrate.

48. A liquid crystal display device which is integrated with a pixel section and drive circuit containing scanning system onto the same substrate, wherein a scan system comprising sampling latch circuit with comparator configuration CMOS latch cell as the basic structure and comprises, a first switch connected respectively between the two input sections and the two input signal sources of said CMOS latch cell and, a second switch connected between the power supply line and the power supply side of said CMOS latch cell and, a control means to control the complementary switching of said first switch and said second switch.

49. A liquid crystal display device as claimed in claim 48, wherein said first switch and said second switch are transistors.

50. A liquid crystal display device as claimed in claim 48, wherein a plurality of said sampling latch circuits are installed and, said second switch is jointly shared by said plurality of sampling latch circuits.

51. A liquid crystal display device as claimed in claim 48 also having a third switch synchronized and controlled by said second switch between the power supply line and the power supply side of the output circuit for output of said CMOS latch circuit output signal.

52. A liquid crystal display device as claimed in claim 51, wherein said second switch is combined with said third switch.

53. A liquid crystal display device as claimed in claim 52, wherein a plurality of said sampling latch circuits are installed corresponding to the number of digital data bits and, said second switch is jointly shared by said plurality of sampling latch circuits.

54. A latch circuit with a CMOS latch cell as a basic structure, wherein said latch circuit has a first switch and a second switch to respectively select a first and second power supply having different voltages and installed on at least one of the positive power side or the negative power side of said CMOS

latch cell and, having a control means to control switching of said first and second switches according to the periods of the latch operation and output operation of said CMOS latch cell.

55. A latch circuit as claimed in claim 54, wherein said first and second switches are transistors.

56. A latch circuit as claimed in claim 54, wherein a plurality of said latch circuits are installed and, said first switch and said second switch are jointly shared by said plurality of sampling latch circuits.

57. A latch circuit as claimed in claim 54, wherein said latch circuit is fabricated by utilizing thin film transistors formed on a glass substrate.

58. A latch circuit as claimed in claim 54, wherein said latch circuit is fabricated by utilizing thin film transistors formed on a silicon substrate.

59. A liquid crystal display device which is integrated with a pixel section and drive circuit containing scanning system on the same substrate, wherein a scan system comprises said CMOS latch cell as the basic structure and comprises, a first switch and a second switch to respectively select a first and second power supply having different voltages and installed on at least one of the positive power side or the negative power side of said CMOS latch cell and, having a control means to control switching of said first and second switches according to the periods of the

latch operation and output operation of said CMOS latch cell.

60. A liquid crystal display device as claimed in claim 59, wherein said first switch and said second switch are transistors.

61. A liquid crystal display device as claimed in claim 59, wherein a plurality of said latch circuits are installed corresponding to the number of digital data bits and, said first switch and said second switch are jointly shared by said plurality of sampling latch circuits.